REMARKS

In the Official Action mailed **May 11, 2001**, the Examiner reviewed claims 1-20. The specification was objected to because of informalities. Claims 1-3, 5-7, and 11-12 were rejected under 35 U.S.C. §102(b) as being anticipated by Dea (USPN 5,469,208, hereinafter "Dea"). Claims 4, 9, 13-17, and 19-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dea in view of Abramatic et al. (USPN 4,546,383, hereinafter "Abramatic"). Claim 8 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dea in view of Hardiman (USPN 5,923,223, hereinafter "Hardiman"). Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dea. Claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dea and Abramatic as applied to claim 13 and further in view of Hardiman.

Related Applications Section

The Examiner objected to the specification because the application number and filing date of the related application were not provided. The related applications section has been amended to include a serial number and a filing date for the related application.

Rejections under 35 U.S.C. §102(e) and §103(a)

Independent claim 1 was rejected as being anticipated by Dea and independent claim 13 was rejected as being unpatentable over Dea in view of Abramatic. Applicant respectfully points out that Dea is directed to a compression/decompression accelerator **coupled to a system bus** (See Dea, Fig. 1). In contrast, the present invention discloses a graphics controller **within a core logic unit** (See Fig. 2, and page 7, line 24 to page 8, line 1 of the instant application). A core logic unit is circuitry within a computer system that interfaces a processor to a memory and a peripheral bus and performs other

functions (See page 5, lines 7-8 of the instant application). Specifically, the core logic unit in the present invention includes the graphics controller and the circuitry of north bridge 118 (see page 7, line 27 of the instant application).

Including the graphics controller into the core logic unit is advantageous because communications between the graphic controller and the core logic elements remain within the core logic unit and are therefore faster than when these communications pass through a system bus. Performing these communications across the system bus is slower because system bus bandwidth is typically less than the bandwidth within the core logic unit, and because of system bus contention with other peripheral devices. There is no suggestion, either explicit or implicit, within Dea, or within Dea in combination with Abramatic, to include the graphics controller within the core logic unit.

Accordingly, Applicant has included the limitations of dependent claims 11 and 20 into independent claims 1 and 13, respectively to clarify that the graphics controller is included within the core logic unit. Independent claims 11 and 20 have been cancelled without prejudice.

Hence, Applicant respectfully submits that independent claims 1-13 as presently amended are in condition for allowance, and that claims 2-10, and 12 which depend upon claim 1, and claims 14-19 which depend on claim 13 are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

Applicant respectfully submits formal drawings to replace the informal drawings. No new matter has been added.

Version with markings to show changes made

From Page 1, Line 13

The subject matter of this application is related to the subject matter in a co-pending non-provisional application by the same inventor as the instant application [and filed on the same day as the instant application]entitled, "Apparatus for Assisting Video Compression in a Computer System," having serial number [TO BE ASSIGNED]09/048,932, and filing date [TO BE ASSIGNED]March 26, 1998[(Attorney Docket No. MEI-97-01386.00)].

The Claims

1. (Once Amended) A method for compressing video data in a computer system, comprising:

receiving a stream of data from a current video frame in the computer system;

computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes computing the difference frame in a core logic chip within the computer system; and

storing the difference frame in a memory in the computer system.

13. (Once Amended) A method for compressing video data in a computer system, comprising:

receiving a stream of data from a current video frame in the computer system;

computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes computing the difference frame in a core logic chip within the computer system;

storing the difference frame in a memory in the computer system;

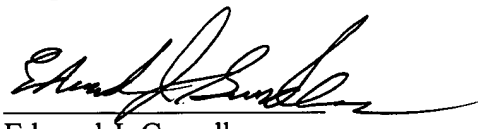
storing the current video frame in the memory in the computer system; and

compressing the video data using the difference frame to produce compressed video data.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 

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Date: August 6, 2001

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